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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/760,560	01/16/2001	Kenny Kok-Hoong Chiu	052404.0098	3810

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EXAMINER	
WILLIAMS, LAWRENCE B	

ART UNIT	PAPER NUMBER
2638	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/760,560	CHIU, KENNY KOK-HOONG	
	Examiner	Art Unit	
	Lawrence B Williams	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 10 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-14,17-22,24-28,30,32-36 and 38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-9,13,14,17-22,27,28,30,32-36 and 38* is/are rejected.

7)☒ Claim(s) *10-12 and 24-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

2. Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has submitted an incomplete claim.

Accordingly, the claim has not been further treated on the merits.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1, 4-5, 14, 17-18, 22, 28, 33-36, 38 are rejected under 35 U.S.C. 102(e) as being anticipated by Miller et al. (US Patent 6,275,546 B1).

(1) With regard to claim 1, Miller et al. discloses in Fig. 1, a clock selection device (10) adapted to select one of a pair of clock sources onto an output clock line, comprising: a first input clock line (20) coupled to a first clock source (CLK A); a second input clock line (28) coupled to a second clock source (CLK B), the second clock source asynchronous to the first clock source (col. 1, line 5; lines 39-41); and a clock selection logic (16) adapted to select from

the first input clock line and the second input clock line, producing an internal clock line coupled to the output clock line; and a clock synchronization logic (12), coupled to the first input clock line, the second input clock line (14), and the clock selection logic, adapted to synchronize the first input clock line, the second input clock line, and the clock selection logic, such that the internal clock line is glitch free (col. 1, lines 63-64), the clock synchronization logic triggering the clock selection logic to select from the first input clock line and the second input clock line (col. 2, lines 37-48) wherein the clock synchronization logic is independent of the internal clock line wherein the first clock source has a first frequency, and wherein the second clock source has a second frequency, the second frequency independent of the first frequency (col. 1, lines 5-7; lines 39-41).

(2) With regard to claim 4, Miller et al. also discloses in Fig. 1, the clock selection device of claim 1, the clock synchronization logic comprising: a first clock synchronization block (12), coupled to the first clock source (CLK A), adapted to synchronize the first clock source and the clock selection logic; and a second clock synchronization block (14), coupled to the second clock source (CLK B), adapted to synchronize the second clock source and the clock selection logic.

(3) With regard to claim 5, Miller et al. also discloses the clock synchronization logic further comprising: a first clock reset signal (64; block 12), synchronized to the first clock signal, adapted to reset the first clock synchronization block; and a second clock reset signal (64, block 14), synchronized to the second clock signal, adapted to reset the second clock synchronization block, wherein the first clock reset signal and the second clock reset signal can be asserted to prevent meta-stability of the clock synchronization logic (col. 3, lines 7-18).

(4) With regard to claim 14, Miller et al. discloses the glitchless clocking circuit relating to computer networking environments which would inherently include a processor-based device comprising: a processor; a plurality of communication controllers coupled to the processor. Furthermore, Miller et al. also discloses in Fig. 1, a first input clock line (20) coupled to the first clock source (CLKA); a second input clock line (28) coupled to the second clock source; and a clock selection logic (16) adapted to select from the first input clock line and the second input clock line, producing an internal clock line; and a clock synchronization logic (12), coupled to the first input clock line, the second input clock line (14), and the clock selection logic, adapted to synchronize the first input clock line, the second input clock line, and the clock selection logic, such that the internal clock line is glitch free (col. 1, lines 63-64), the clock synchronization logic triggering the clock selection logic to select from the first input clock line and the second input clock line (col. 2, lines 37-48), wherein the clock synchronization logic is independent of the internal clock line, wherein the first clock source has a first frequency, and wherein the second clock source has a second frequency, the second frequency independent of the first frequency (col. 1, lines 5-7; lines 39-41).

(5) With regard to claim 17, claim 17 inherits all limitations of claim 14 above. Furthermore, Miller et al. also discloses in Fig. 1, the clock selection device of claim 1, the clock synchronization logic comprising: a first clock synchronization block (12), coupled to the first clock source (CLK A), adapted to synchronize the first clock source and the clock selection logic; and a second clock synchronization block (14), coupled to the second clock source (CLK B), adapted to synchronize the second clock source and the clock selection logic.

(6) With regard to claim 18, claim 18 inherits all limitations of claim 14 above. Furthermore, Miller et al. also discloses the clock synchronization logic further comprising: a first clock reset signal (64; block 12), synchronized to the first clock signal, adapted to reset the first clock synchronization block; and a second clock reset signal (64, block 14), synchronized to the second clock signal, adapted to reset the second clock synchronization block, wherein the first clock reset signal and the second clock reset signal can be asserted to prevent meta-stability of the clock synchronization logic (col. 3, lines 7-18).

(7) With regard to claim 22, Miller et al. also discloses the clock selection device further comprising: a clock selection signal, asynchronous to the first clock source and the second clock source, adapted to cause the clock selection logic to select one of the first input clock source and the second input clock source onto the internal clock line, selecting the first input clock source when the clock selection signal is asserted and the second input clock source when the clock selection signal is unasserted (col. 2, lines 14-17).

(8) With regard to claim 28, claim 28 discloses limitations of a method of device and apparatus claims 1 and 14. Therefore a similar rejection applies.

(9) With regard to claim 33, claim 33 discloses limitations similar to those disclosed in claim 18. Therefore a similar rejection applies.

(10) With regard to claim 34, claim 34 inherits all limitations of claim 28 above. Furthermore, Miller et al. also discloses the method of claim 28, step (c) comprising the steps of:
(c1) receiving a clock select signal asynchronous to the first clock signal and the second clock signal; and
(c2) connecting the first clock signal to the output clock line when the clock select signal is asserted;
(c3) connecting the second clock signal to the output clock line when the clock select signal is deasserted;

step (d) comprising the step of: (d) synchronizing the first input clock signal, the second input clock signal, and steps (c2) and (c3), such that the output clock line is glitch free (col. 2, lines 36-56).

(11) With regard to claim 35, claim 35 discloses limitations similar to those of claims 1 and 14. Therefore a similar rejection applies.

(12) With regard to claim 36, claim 36 inherits all limitations of claim 35 above. Furthermore, Miller et al. also discloses the clock synchronization logic further comprising: a first clock reset signal (64; block 12), synchronized to the first clock signal, adapted to reset the first clock synchronization block; and a second clock reset signal (64, block 14), synchronized to the second clock signal, adapted to reset the second clock synchronization block, wherein the first clock reset signal and the second clock reset signal can be asserted to prevent meta-stability of the clock synchronization logic (col. 3, lines 7-18).

(13) With regard to claim 38, Miller et al. also discloses in Fig. 1, a first synchronization means (12) coupled to the first clock source for synchronizing the first clock source (CLKA) to the clock switching means (16); a second synchronization means (14) coupled to the second clock source for synchronizing the second clock source (CLKB) to the clock switching means; a clock selection means (16) coupled to the first synchronization means and the second synchronization means for causing the clock switching means to switch between the first clock source and the second clock source; a first feedback (54) means coupled to the clock selection means and the first synchronization means for synchronizing the second synchronization means and the dock selection means; and a second feedback means (44) coupled to the clock selection means and the second synchronization means for synchronizing the first synchronization means and the clock selection means.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (US Patent 6,275,546 B1) as applied to claims 1 and 14 above, in view of Szczepanek (US Patent 5,517,638).

(1) With regard to claim 6, claim 6 inherits all limitations of claim 1 above. Miller et al. discloses all limitations of claim 1 above. Miller et al. does not however disclose the clock synchronization logic is scalable to produce a predetermined delay time between the assertion of the clock select signal and the selection onto the output line by the clock selection logic.

However, Szczepanek teaches a clock synchronization logic scalable to produce a predetermined delay time between the assertion of the clock select signal and the selection onto the output line by the clock selection logic (col. 6, lines 61-64).

It would have been obvious to one skilled in the art at the time of the invention to incorporate the teachings of Szczepanek with the invention of Miller et al. as a method of producing different preselected delays in the circuitry.

(2) With regard to claim 19, claim 19 discloses limitations similar to those of claim 6 above. Therefore a similar rejection applies.

7. Claims 7, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (US Patent 6,275,546 B1) as applied to claims 1 and 14 above, in view of Swoboda (US Patent 5,790,609).

(1) With regard to claim 7, claim 7 inherits all limitations of claim 1 above. As noted above, Miller et al. discloses all limitations of claims 1 and 14 above. Miller et al. does not however teach, wherein the clock selection logic comprises a multiplexer with two clock input lines.

However, Swoboda teaches in Fig(s). 1, 2, wherein a clock selection logic comprises a multiplexer with two clock input lines.

It would have been obvious to one skilled in the art at the time of the invention to incorporate the teachings of Swoboda with the invention of Miller et al. as a method of providing glitchless switching between asynchronous clock sources (col. 1, lines 58-64).

(2) With regard to claim 20, claim 20 discloses limitations similar to those of claim 7 above. Therefore a similar rejection applies.

8. Claims 8, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (US Patent 6,275,546 B1) as applied to claims 7, 20 above, in view of Swoboda (US Patent 5,790,609) and further in view of Schwake (US Patent 6,782,064 B1).

(1) With regard to claim 8, claim 8 inherits all limitations of claim 7 above. As noted above, Miller et al. in combination with Swoboda disclose all limitations of claim 7. They do not however disclose wherein the multiplexer switches only when both clock input lines of the multiplexer are at the same assertion level. However Schwake discloses switching logic that

switches only when both clock input lines of the logic are at the same assertion level (col. 8, lines 1-11).

It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Schwake with the invention of Miller et al. in combination with Swoboda as a method of preventing clock-induced glitches.

(2) With regard to claim 21, claim 21 discloses limitations similar to those disclosed in claim 8 above. Therefore a similar rejection applies.

9. Claims 13, 27, 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (US Patent 6,275,546 B1) as applied to claims 1, 14 above, in view of Watt (US Patent 5,675,615).

(1) With regard to claim 13, as noted above, Miller et al. discloses all limitations of claim 1 above. Miller et al. does not however disclose a buffer connected to the internal clock line, producing a buffered output clock signal.

However, Watt discloses a buffer connected to the internal clock line, producing a buffered output clock signal.

It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Watt with the invention of Miller et al. as a method of temporarily storing the selected output clock signal.

(2) With regard to claim 27, claim 27 discloses limitations similar to those of claim 13 above. Therefore a similar rejection applies.

(3) With regard to claim 30, claim 30 discloses limitations similar to those of claims 13 and 27 above. Therefore a similar rejection applies.

10. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (US Patent 6,275,546 B1) as applied to claim 28 above, in view of Schwake (US Patent 6,782,064 B1).

As noted above, Miller et al. discloses all limitations of claim 28. Miller et al. does not however disclose delaying step (c) for a predetermined amount of time.

However, Schwake discloses delaying the step (c) for a predetermined amount of time (col. 8, lines 1-11).

It would have been obvious to one skilled in the art at the time of invention to combine the teachings of Schwake with the teachings of Miller et al. as method of prevent clock-induced glitches.

Allowable Subject Matter

11. Claims 10-12, 24-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a.) Wilcox discloses in US Patent 6,738,442 B1 Pulse Detection And Synchronization System.

b.) Goodnow discloses in US Patent 6,107,841 Synchronous Clock Switching Circuit For Multiple Asynchronous Clock Source.

c.) Shen discloses in US Patent 6,310,822 B1 Delay Locking High Speed Clock Synchronous Method And Circuit.

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence B Williams whose telephone number is 571-272-3037. The examiner can normally be reached on Monday-Friday (8:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on 571-272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lawrence B. Williams

lbw
October 23, 2005

EMMANUEL BAYARD
PRIMARY EXAMINER